Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (original) A method comprising:

installing a timer by writing a status bit into a first table indexed by a first pointer, and writing a value corresponding to timer information into a second table indexed by the first pointer.

2. (original) The method of claim 1 wherein the value comprises a memory address of a connection descriptor structure.

3. (original) The method of claim 1 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

4. (original) The method of claim 1 further comprising:

canceling the timer by changing the status bit.

5. (original) The method of claim 1 further comprising:

sending the value to a process to expire the timer.

6. (original) The method of claim 1 wherein expiring the timer comprises:

reading the value;

determining whether the status bit has been changed; and

sending a message including the value to expire the timer if the status has not been changed.

7. (original) The method of claim 1 further comprising:

incrementing the first pointer and a second pointer based on a clock.

8. (original) The method of claim 1 wherein expiring the timer further comprises:

incrementing the second pointer; and

incrementing the first pointer if a difference between the first pointer and the second pointer is smaller than a pre-determined offset.

9. (original) The method of claim 1 wherein reading the value includes reading other values in the second table adjacent to the value.

10. (withdrawn) A method comprising:

installing a number of timers during a first time interval; and

expiring a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.

11. (withdrawn) The method of claim 10 wherein the timers have the same expiration time.

12. (withdrawn) The method of claim 10 wherein expiring a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval comprises

expiring the first one of the timers during the second time interval if the first one of the timers was one of the first N timers to be installed during the first time interval, or expiring the first one of the timers during the third time interval otherwise, where N is a pre-determined number.

13. (currently amended) A computer program product tangibly embodied on a ~~computer~~ machine readable ~~medium~~ storage device, for managing timers, comprising instructions for causing a computer to:

install a timer by writing a status bit into a first table indexed by a first pointer, and writing a value corresponding to timer information into a second table indexed by the first pointer.

14. (original) The computer program product of claim 13 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

15. (original) The computer program product of claim 13 further comprising instructions for causing the computer to:

cancel the timer by changing the status bit.

16. (original) The computer program product of claim 13 further comprising instructions for causing the computer to:

send the value to a process to expire the timer.

17. (original) A system comprising:

a host including an input port for receiving data packets and an output port for transmitting data packets;

a memory structure; and

a processor associated with the memory structure the processor configured to

install a timer by writing a status bit into a first table in memory, the first table indexed by a first pointer, and write a value corresponding to timer information into a second table in memory, the second table indexed by the first pointer.

18. (original) The system of claim 17 wherein the processor comprises a microengine array.

19. (original) The system of claim 17 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

20. (original) The system of claim 17 wherein the processor is further configured to cancel the timer by changing the status bit.

21. (original) The system of claim 17 wherein the processor is further configured to send the value to a process to expire the timer.

22. (withdrawn) A computer program product tangibly embodied on a computer readable medium, for managing timers, comprising instructions for causing a computer to:

install a number of timers during a first time interval; and

expire a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.

23. (withdrawn) The computer program product of claim 22 wherein the timers have the same expiration time.

24. (withdrawn) The computer program product of claim 22 wherein expiring a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval comprises

expiring the first one of the timers during the second time interval if the first one of the timers was one of the first N timers to be installed during the first time interval, or expiring the first one of the timers during the third time interval otherwise, where N is a pre-determined number.

25. (withdrawn) A system comprising:

a host including an input port for receiving data packets and an output port for transmitting data packets;

a memory structure; and

a processor associated with the memory structure the processor configured to

installing in memory a number of timers during a first time interval; and

expiring a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.

26. (withdrawn) The system of claim 25 wherein the timers have the same expiration time.

27. (withdrawn) The system of claim 25 wherein expiring a first one of the timers during either a second time interval or a third time interval based on the number of timers installed during the first time interval comprises

expiring the first one of the timers during the second time interval if the first one of the timers was one of the first N timers to be installed during the first time interval, or expiring the first one of the timers during the third time interval otherwise, where N is a pre-determined number.

28. (original) A processor comprising:

circuitry configured to

install a timer by writing a status bit into a first table in a memory, the first table indexed by a first pointer, and write a value corresponding to timer information into a second table in memory, the second table indexed by the first pointer.

29. (original) The processor of claim 28 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

30. (original) The processor of claim 28 wherein the processor is further configured to cancel the timer by changing the status bit.

31. (currently amended) A system comprising:

a network host having a network processor;

a ~~TCP~~ Transmission Control Protocol (TCP) offload engine in communication with the network processor; and

a wireless ~~PHY~~ device in communication with the network processor;

wherein the TCP offload engine is configured to

install a timer by writing a status bit into a first table in a memory, the first table indexed by a first pointer, and write a value corresponding to timer information into a second table in memory, the second table indexed by the first pointer.

32. (original) The system of claim 31 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

33. (original) The system of claim 31 wherein the TCP offload engine is further configured to cancel the timer by changing the status bit.

34. (original) A method comprising:

receiving a first data packet from a source;

installing a timer by writing a status bit into a first table in a memory, the first table indexed by a first pointer, and writing a value corresponding to timer information into a second table in memory, the second table indexed by the first pointer; and

sending a second data packet to the source for acknowledging receipt of the first data packet, after the timer has expired.

35. (original) The method of claim 34 wherein the first table stores a plurality of status bits including the status bit and the second table stores a plurality of values corresponding to a like plurality of timers.

36. (original) The method of claim 34 further comprising canceling the timer by changing the status bit.